

**3.5A/2.5A, 30V, 0.060/0.150 Ohms,  
Complementary LittleFET™ Power  
MOSFET**

The RF1K49224 complementary power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This device can be operated directly from integrated circuits.

Formerly developmental type TA49224.

**Ordering Information**

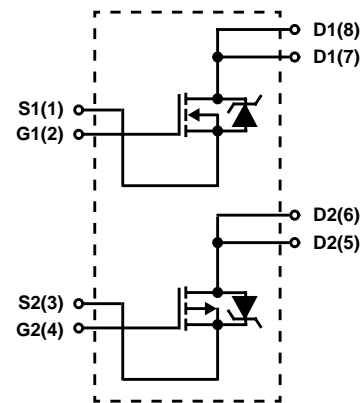
PART NUMBER	PACKAGE	BRAND
RF1K49224	MS-012AA	RF1K49224

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4922496.

**Features**

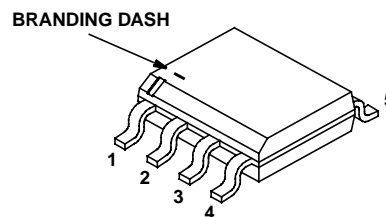
- 3.5A, 30V (N-Channel)  
2.5A, 30V (P-Channel)
- $r_{DS(ON)} = 0.060\Omega$  (N-Channel)  
 $r_{DS(ON)} = 0.150\Omega$  (P-Channel)
- Temperature Compensating PSPICE® Model
- Thermal Impedance PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



**Packaging**

**JEDEC MS-012AA**



# RF1K49224

## Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

	N-CHANNEL	P-CHANNEL	UNITS
Drain to Source Voltage . . . . . $V_{DSS}$	30	-30	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) . . . . . $V_{DGR}$	30	-30	V
Gate to Source Voltage . . . . . $V_{GS}$	$\pm 20$	$\pm 20$	V
Drain Current			
Continuous (Pulse Width = 5s) . . . . . $I_D$	3.5	2.5	A
Pulsed . . . . . $I_{DM}$	Refer to Peak Current Curve	Refer to Peak Current Curve	
Pulsed Avalanche Rating . . . . . $E_{AS}$	Refer to UIS Curve	Refer to UIS Curve	
Power Dissipation . . . . . $P_D$	2	2	W
Derate Above $25^\circ\text{C}$ . . . . .	0.016	0.016	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature . . . . . $T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s . . . . . $T_L$	300	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . . $T_{pkg}$	260	260	$^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

## N-Channel Electrical Specifications $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V	
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	-	3	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	$T_A = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
			$T_A = 150^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	100	nA	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 3.5\text{A}$	$V_{GS} = 10\text{V}$	-	-	0.060	$\Omega$
			$V_{GS} = 4.5\text{V}$			0.132	$\Omega$
Turn-On Time	$t_{ON}$	$V_{DD} = 15\text{V}, I_D \cong 3.5\text{A}, R_L = 4.29\Omega, V_{GS} = 10\text{V}, R_{GS} = 25\Omega$	-	-	50	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	10	-	ns	
Rise Time	$t_r$		-	30	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	60	-	ns	
Fall Time	$t_f$		-	45	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	130	ns	
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V to } 20\text{V}$	$V_{DD} = 24\text{V}, I_D \cong 3.5\text{A}, R_L = 6.86\Omega, I_{g(REF)} = 1.0\text{mA}$	-	35	45	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0\text{V to } 10\text{V}$		-	13	17	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V to } 2\text{V}$		-	2.3	2.9	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	575	-	pF	
Output Capacitance	$C_{OSS}$		-	275	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	100	-	pF	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material	-	-	62.5	$^\circ\text{C}/\text{W}$	

## N-Channel Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 3.5\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 3.5\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	45	ns

**P-Channel Electrical Specifications**  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	-30	-	-	V	
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	-1	-	-3	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\text{V}$ , $V_{GS} = 0\text{V}$	$T_A = 25^\circ\text{C}$	-	-	-1	$\mu\text{A}$
			$T_A = 150^\circ\text{C}$	-	-	-50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	100	nA	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 2.5\text{A}$	$V_{GS} = -10\text{V}$	-	-	0.150	$\Omega$
			$V_{GS} = -4.5\text{V}$	-	-	0.360	$\Omega$
Turn-On Time	$t_{ON}$	$V_{DD} = -15\text{V}$ , $I_D \cong 2.5\text{A}$ , $R_L = 6\Omega$ , $V_{GS} = -10\text{V}$ , $R_{GS} = 25\Omega$	-	-	40	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	9	-	ns	
Rise Time	$t_r$		-	19	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	60	-	ns	
Fall Time	$t_f$		-	34	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	-	140	ns
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0\text{V to } -20\text{V}$	$V_{DD} = -24\text{V}$ , $I_D \cong 2.5\text{A}$ , $R_L = 9.6\Omega$ $I_{g(REF)} = -1.0\text{mA}$	-	28	35	nC
Gate Charge at -10V	$Q_g(-10)$	$V_{GS} = 0\text{V to } -10\text{V}$		-	15	19	nC
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V to } -2\text{V}$		-	1.5	1.9	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = -25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	580	-	pF	
Output Capacitance	$C_{OSS}$		-	260	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	38	-	pF	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material	-	-	62.5	$^\circ\text{C/W}$	

**P-Channel Source to Drain Diode Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = -2.5\text{A}$	-	-	-1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = -2.5\text{A}$ , $dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	49	ns

**Typical Performance Curves (N-Channel)**

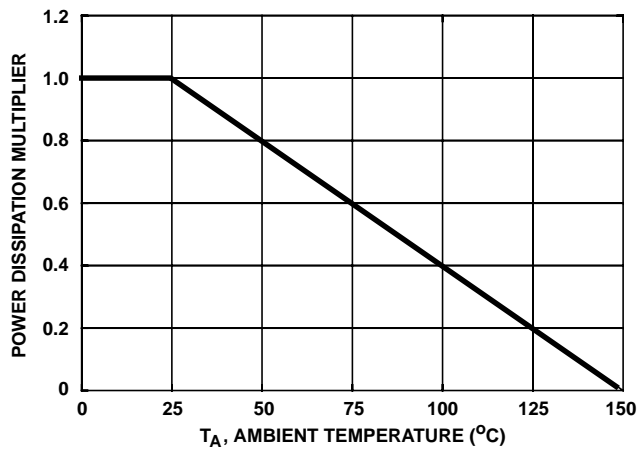


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

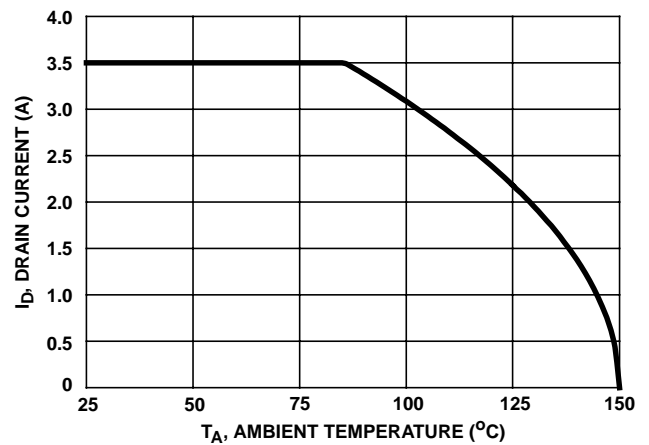


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves (N-Channel) (Continued)

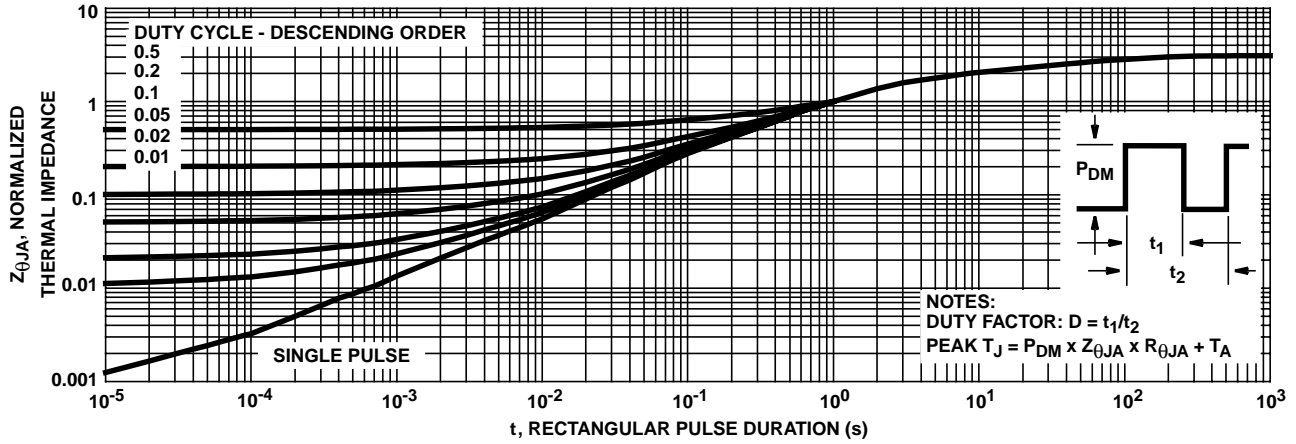


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

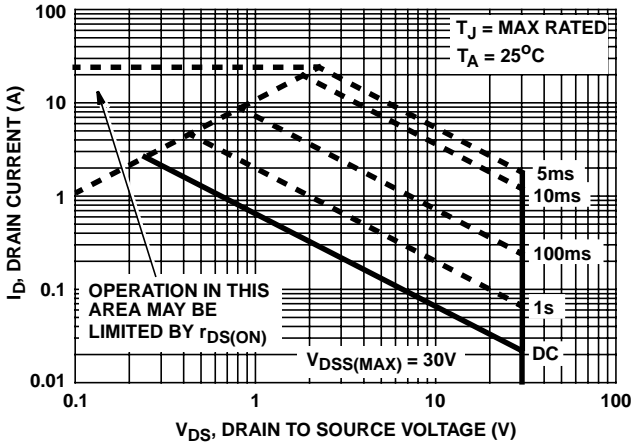


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

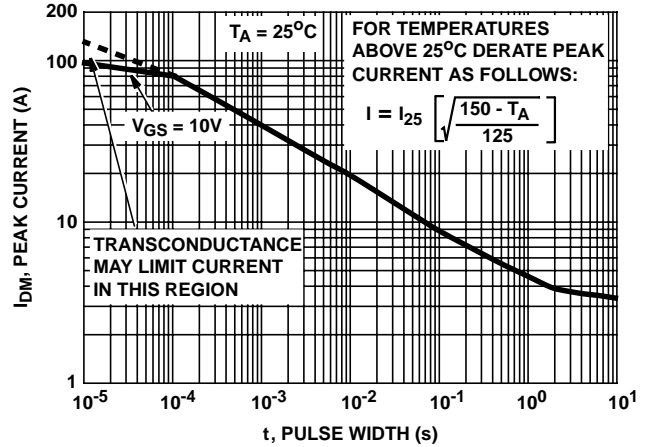
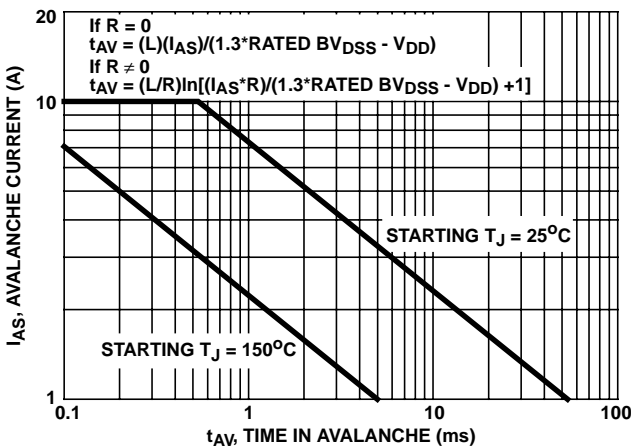


FIGURE 5. PEAK CURRENT CAPABILITY



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

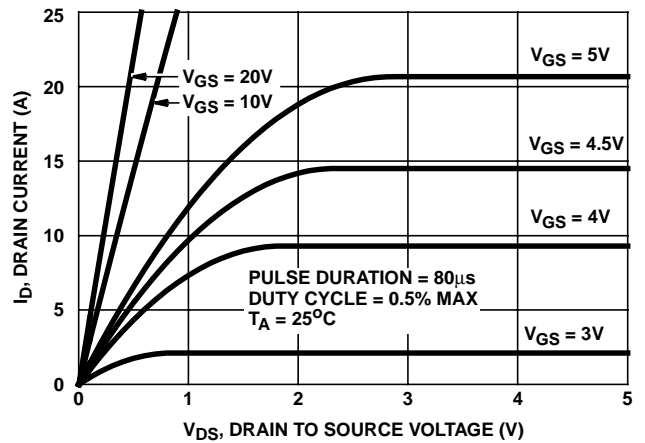


FIGURE 7. SATURATION CHARACTERISTICS

Typical Performance Curves (N-Channel) (Continued)

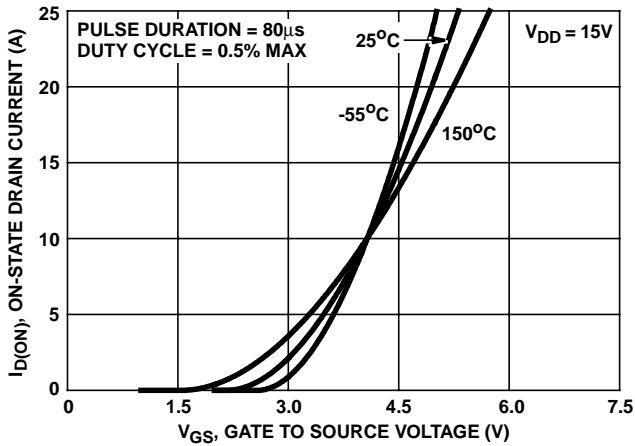


FIGURE 8. TRANSFER CHARACTERISTICS

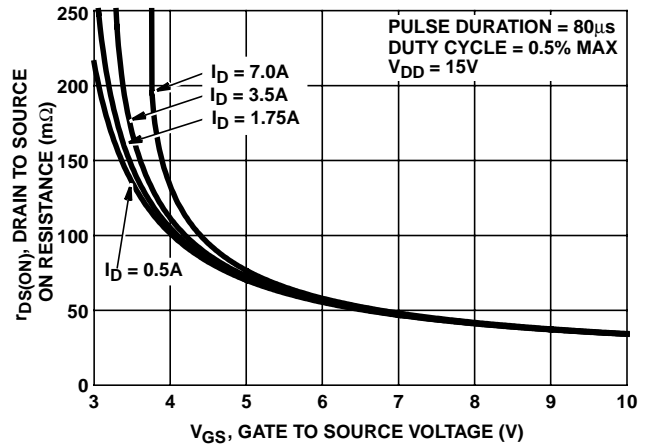


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

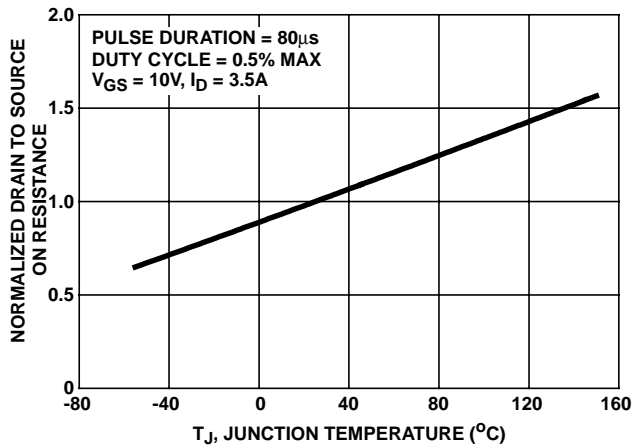


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

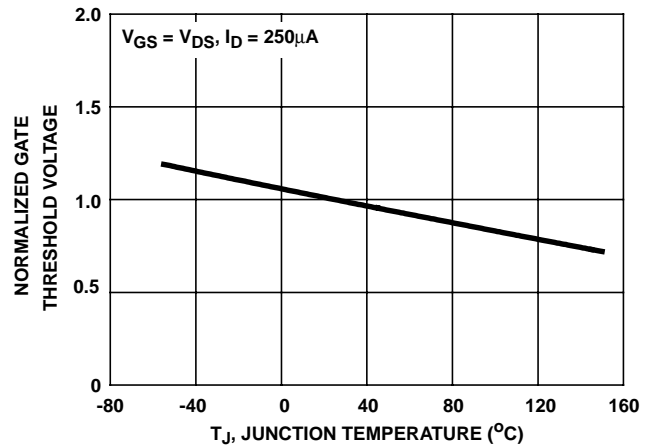


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

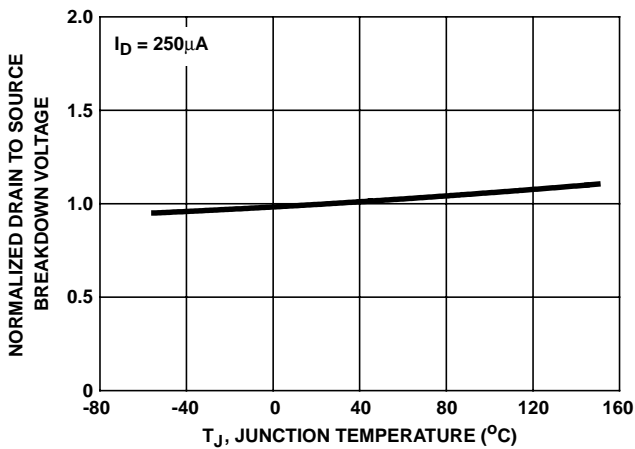


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

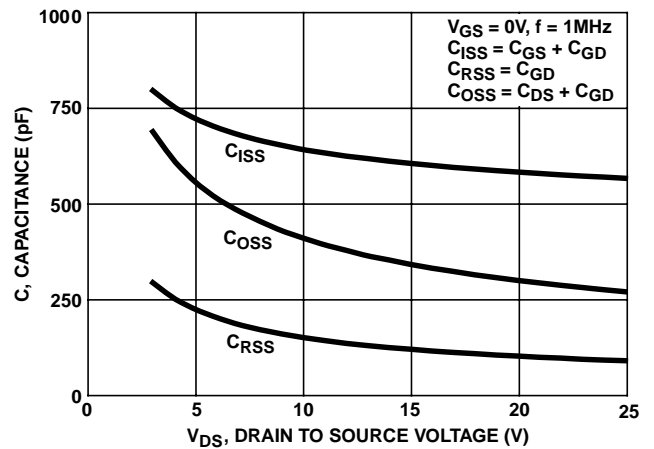
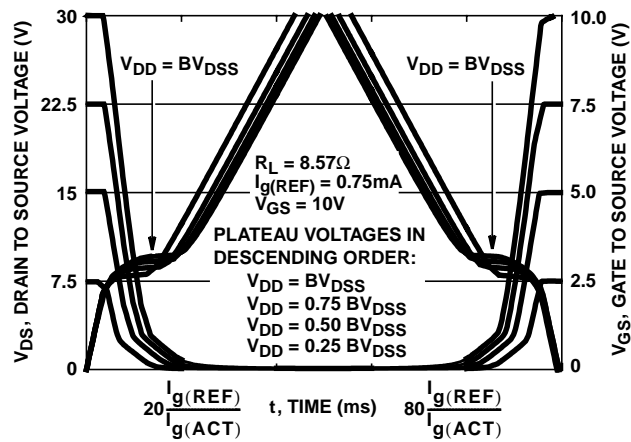


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (N-Channel) (Continued)



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms (N-Channel)

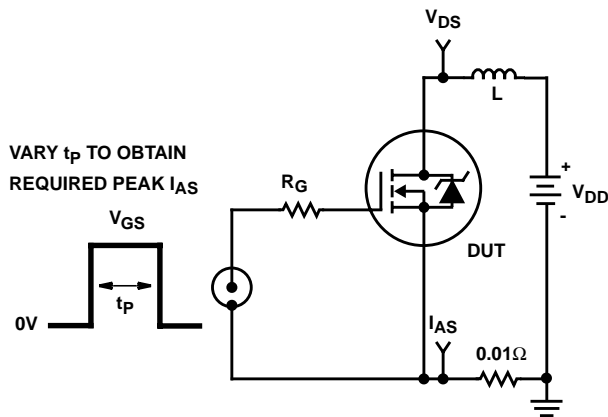


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

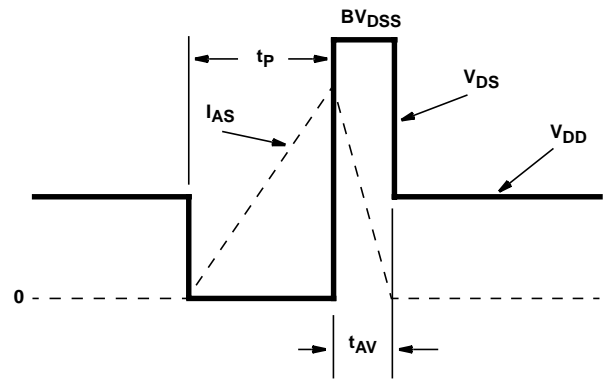


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

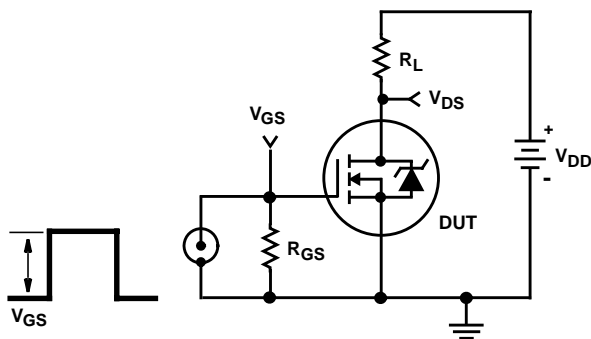


FIGURE 17. SWITCHING TIME TEST CIRCUIT

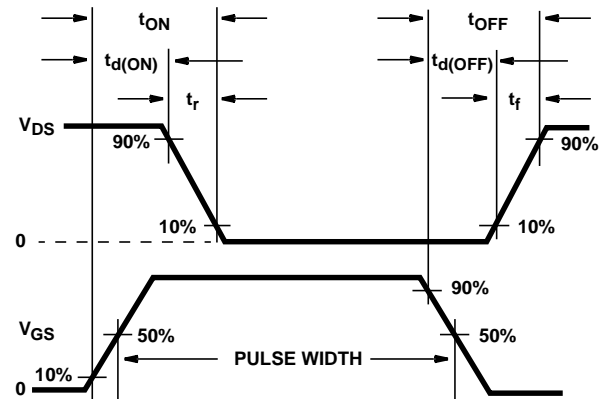


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (N-Channel) (Continued)

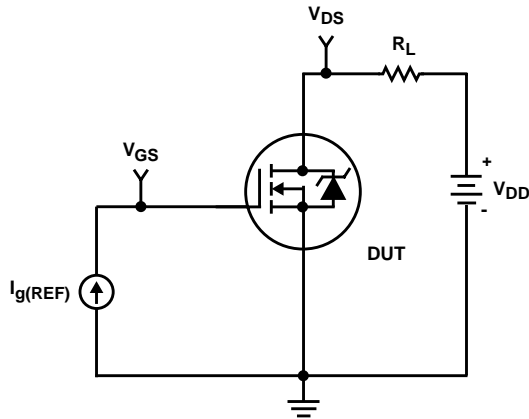


FIGURE 19. GATE CHARGE TEST CIRCUIT

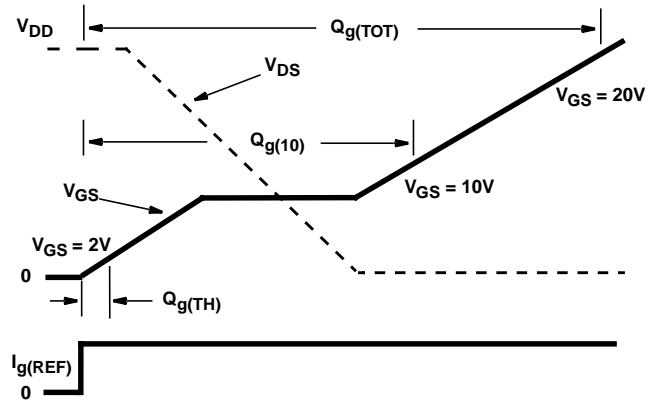


FIGURE 20. GATE CHARGE WAVEFORM

Typical Performance Curves (P-Channel)

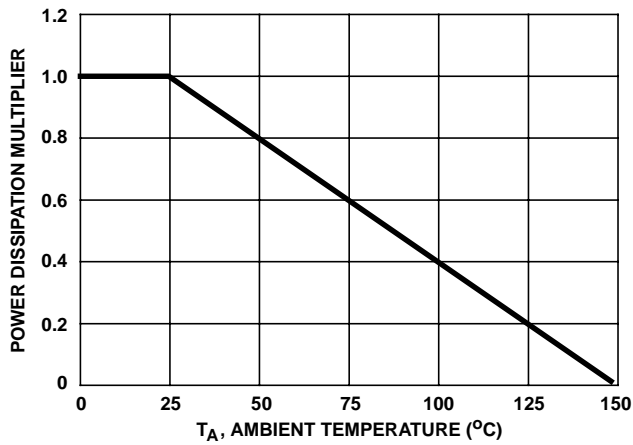


FIGURE 21. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

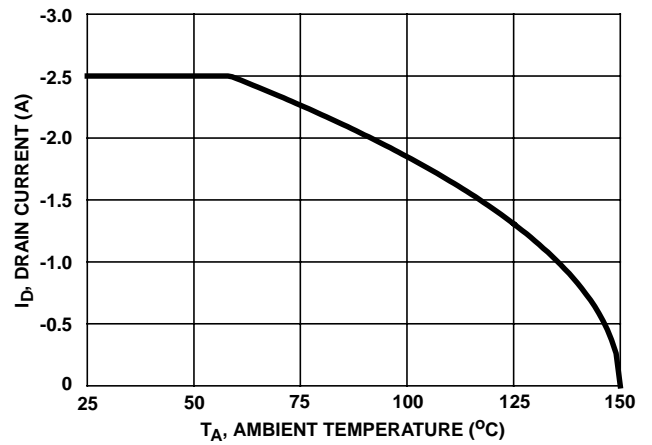


FIGURE 22. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

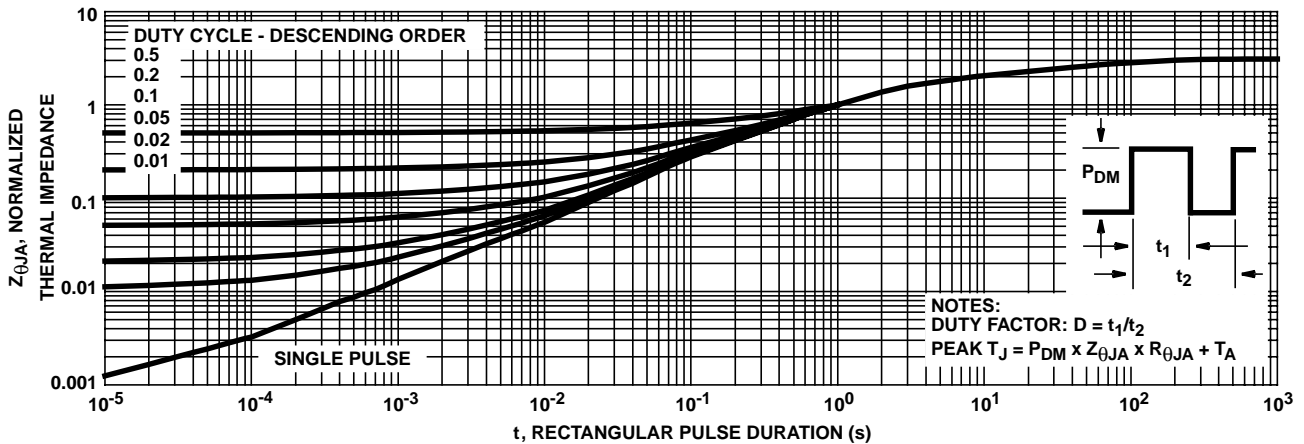


FIGURE 23. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (P-Channel) (Continued)

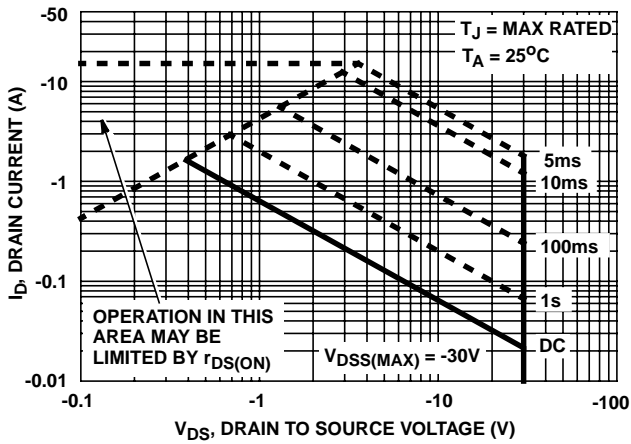


FIGURE 24. FORWARD BIAS SAFE OPERATING AREA

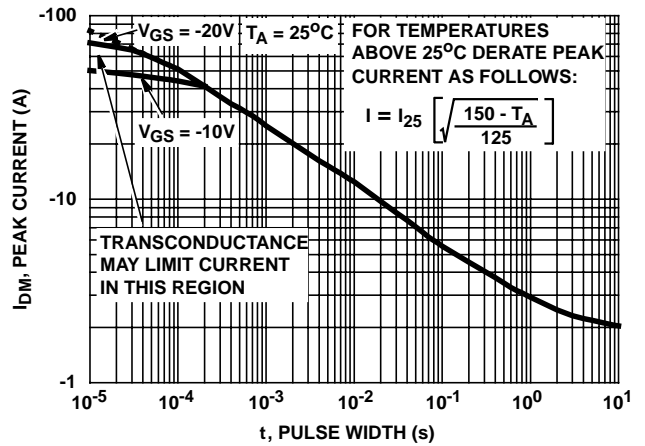
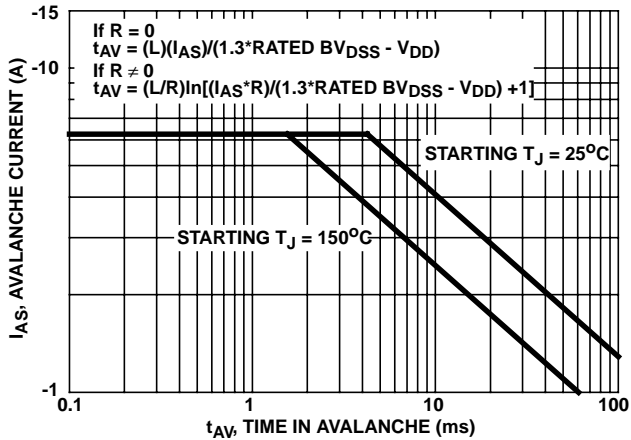


FIGURE 25. PEAK CURRENT CAPABILITY



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 26. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

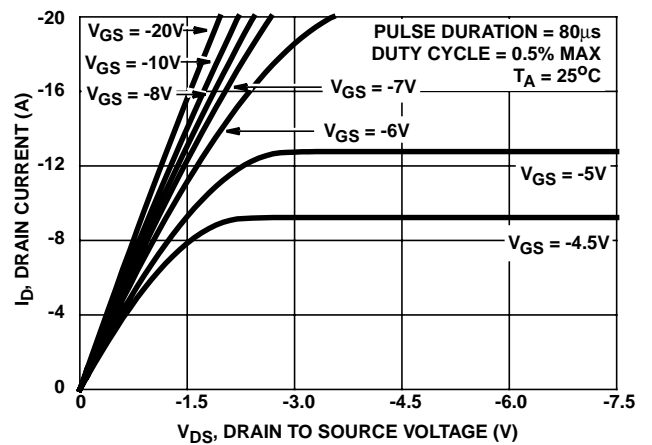


FIGURE 27. SATURATION CHARACTERISTICS

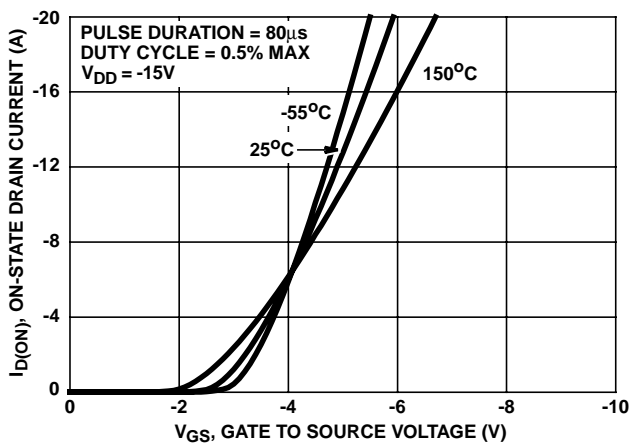


FIGURE 28. TRANSFER CHARACTERISTICS

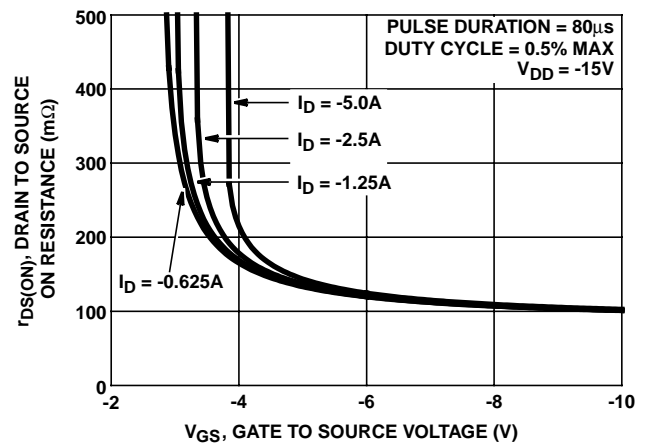


FIGURE 29. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT



Typical Performance Curves (P-Channel) (Continued)

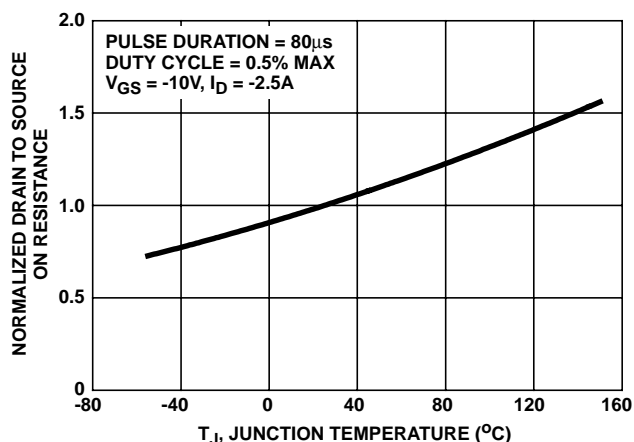


FIGURE 30. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

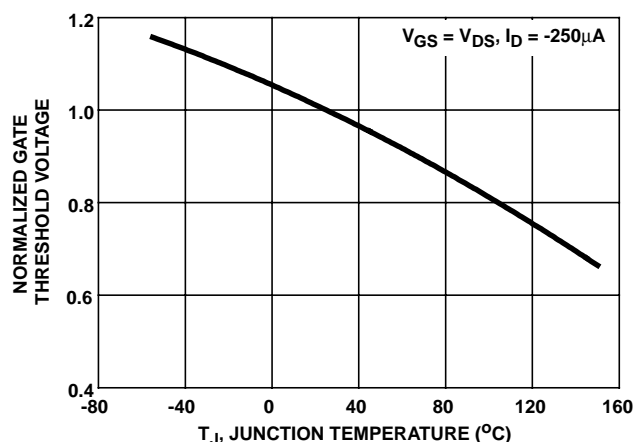


FIGURE 31. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

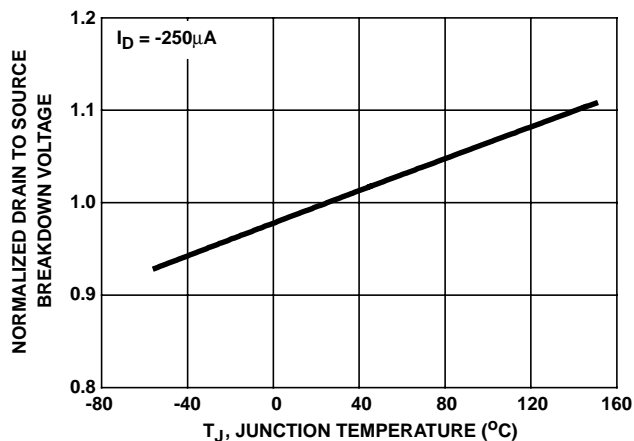


FIGURE 32. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

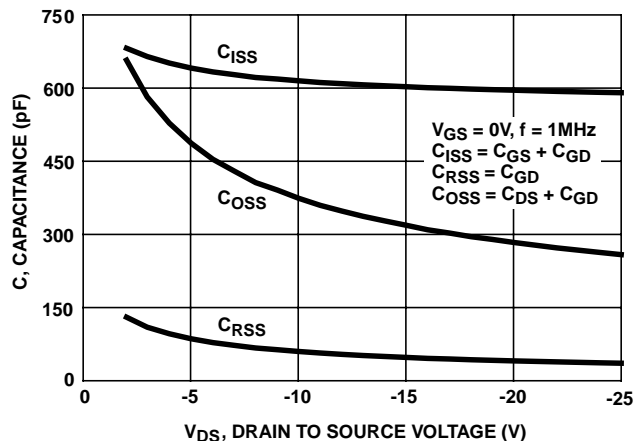
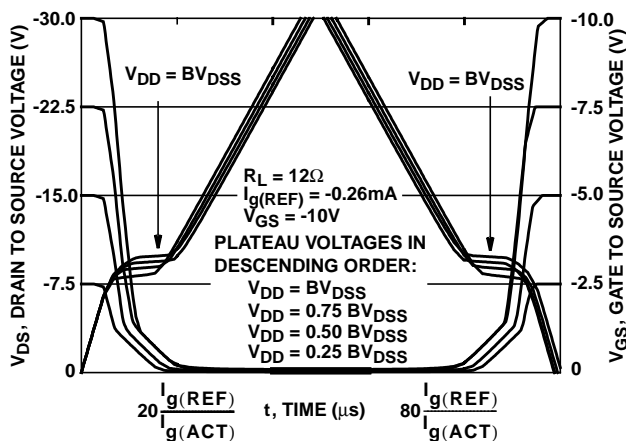


FIGURE 33. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 34. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms (P-Channel)

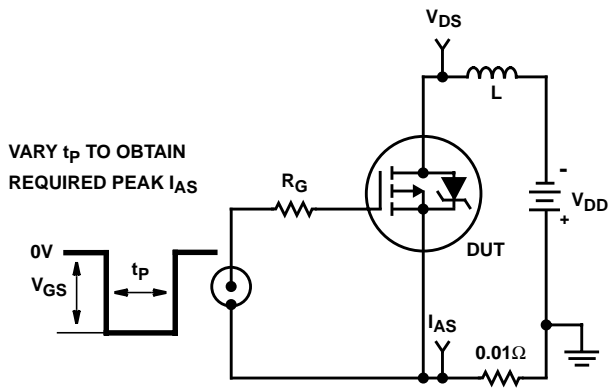


FIGURE 35. UNCLAMPED ENERGY TEST CIRCUIT

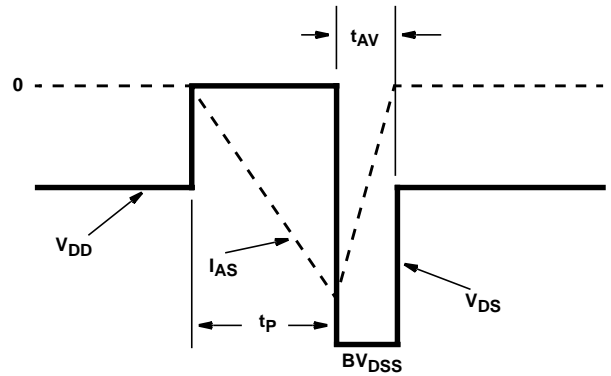


FIGURE 36. UNCLAMPED ENERGY WAVEFORMS

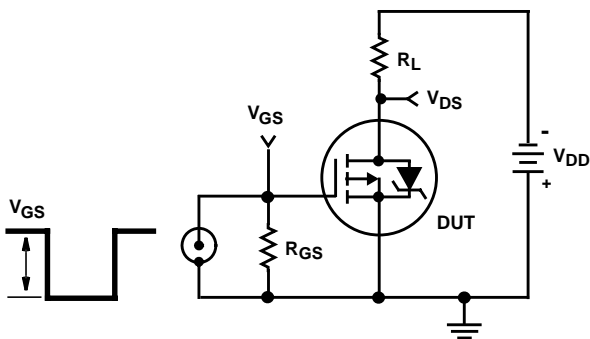


FIGURE 37. SWITCHING TIME TEST CIRCUIT

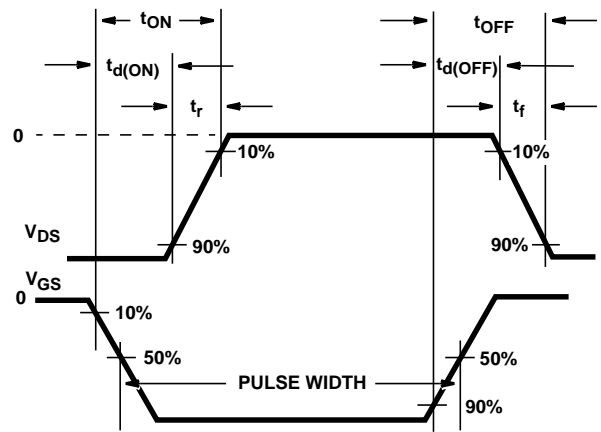


FIGURE 38. RESISTIVE SWITCHING WAVEFORMS

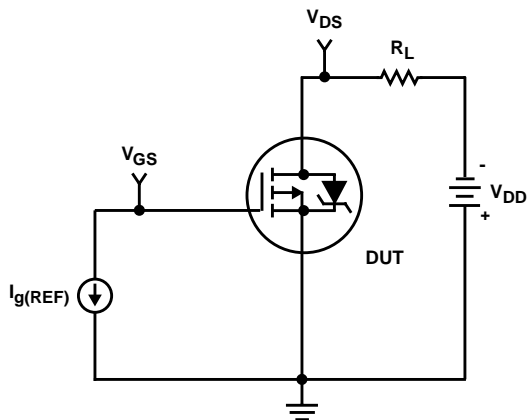


FIGURE 39. GATE CHARGE TEST CIRCUIT

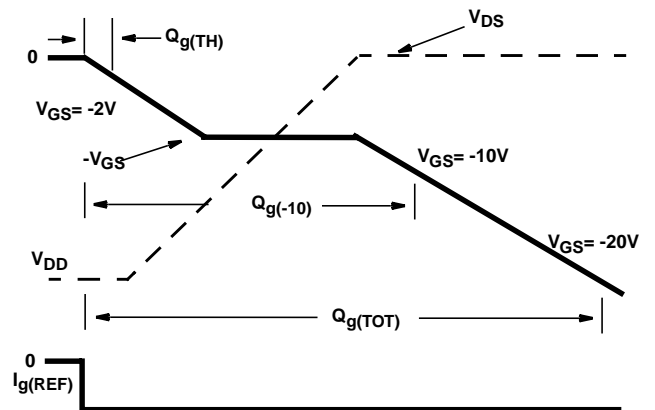


FIGURE 40. GATE CHARGE WAVEFORMS

## **Soldering Precautions**

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

**PSPICE Electrical Model (N-Channel)**

SUBCKT RF1K49224 2 1 3 ; N-Channel Model rev 12/15/94

CA 12 8 1.75e-9  
 CB 15 14 1.80e-9  
 CIN 6 8 1.20e-9

DBODY 7 5 DBDMOD  
 DBREAK 5 11 DBKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.29  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTO 20 6 18 8 1

IT 8 17 1

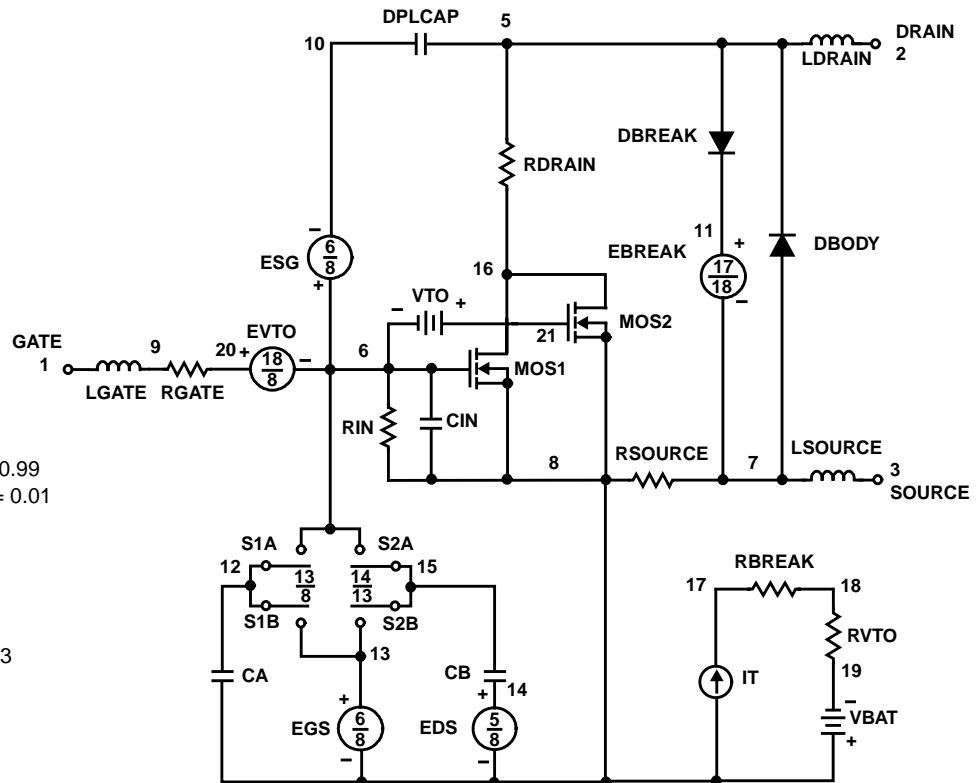
LDRAIN 2 5 1e-9  
 LGATE 1 9 1.233e-9  
 LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99  
 MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1  
 RDRAIN 5 16 RDSMOD 1e-4  
 RGATE 9 20 1.83  
 RIN 6 8 1e9  
 RSOURCE 8 7 RDSMOD 13.5e-3  
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1  
 VTO 21 6 0.1



.MODEL DBDMOD D (IS = 2.50e-13 RS = 1.35e-2 TRS1 = 4.31e-5 TRS2 = 2.15e-5 CJO = 9.33e-10 TT = 2.08e-8)  
 .MODEL DBKMOD D (RS = 1.14 TRS1 = 2.23e-3 TRS2 = -8.91e-6)  
 .MODEL DPLCAPMOD D (CJO = 7.99e-10 IS = 1e-30 N = 10)  
 .MODEL MOSMOD NMOS (VTO = 2.15 KP = 6.25 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL RBKMOD RES (TC1 = 7.74e-4 TC2 = 1.13e-6)  
 .MODEL RDSMOD RES (TC1 = 4.5e-3 TC2 = -7.45e-7)  
 .MODEL RVTOMOD RES (TC1 = -4.16e-3 TC2 = 2.16e-6)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.15 VOFF = -5.15)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.15 VOFF = -7.15)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.6 VOFF = 2.4)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.4 VOFF = -2.6)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

**PSPICE Electrical Model (P-Channel)**

SUBCKT RF1K49224 2 1 3 ; P-Channel Model rev 4/7/97

CA 12 8 7.29e-10  
 CB 15 14 5.01e-10  
 CIN 6 8 5.55e-10

DBODY 5 7 DBODYMOD  
 DBREAK 7 11 DBREAKMOD  
 DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -35.46  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 5 10 8 6 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 6 20 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 1.27e-9  
 LSOURCE 3 7 4.20e-10

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 19.3e-3  
 RGATE 9 20 7.44  
 RLDRAIN 2 5 10  
 RLGATE 1 9 12.7  
 RLSOURCE 3 7 4.2  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 65.37e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

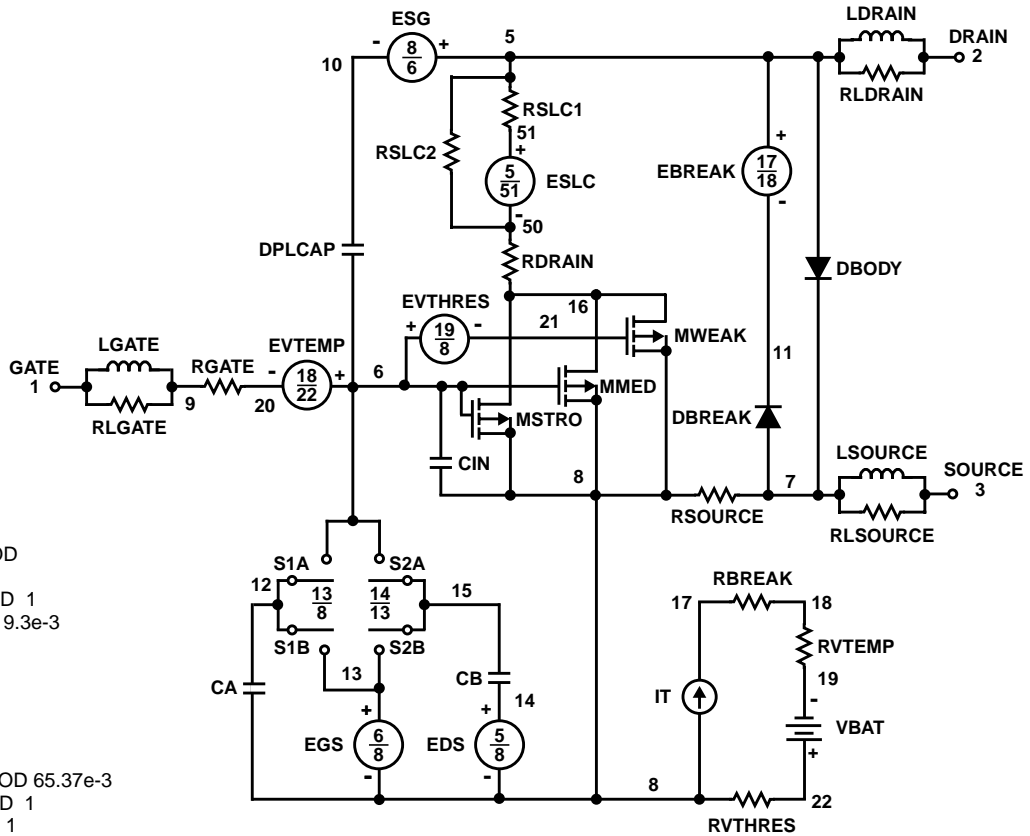
VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*48),2.5))}

```
.MODEL DBODYMOD D (IS = 3.30e-13 RS = 4.56e-2 TRS1 =6.98e-4 TRS2 =8.08e-7 CJO = 8.21e-10 TT = 3.51e-8 M=0.4)
.MODEL DBREAKMOD D (RS = 8.18e-1 TRS1 =5.28e-3 TRS2 = -7.18e-5)
.MODEL DPLCAPMOD D (CJO = 2.52e-10 IS = 1e-30 N = 10 M=0.6)
.MODEL MMEDMOD PMOS (VTO= -1.95 KP=0.75 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=7.44)
.MODEL MSTROMOD PMOS (VTO= -2.44 KP= 7.25 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MWEAKMOD PMOS (VTO= -1.68 KP=0.045 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=74.4 RS=0.1)
.MODEL RBREAKMOD RES (TC1 = 9.45e-4 TC2 = -1.01e-7)
.MODEL RDRAINMOD RES (TC1 = 3.69e-3 TC2 = 5.90e-6)
.MODEL RSLCMOD RES (TC1=3.46e-3 TC2= 1.26e-6)
.MODEL RSOURCEMOD RES (TC1=3.69e-3 TC2=5.90e-6)
.MODEL RVTHRESMOD RES (TC=-5.19e-4 TC2= 5.02e-6)
.MODEL RVTEMPMOD RES (TC1 = -3.54e-3 TC2 = -6.53e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 6.94 VOFF= 3.94)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.94 VOFF= 6.94)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.40 VOFF= -2.60)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.60 VOFF= 0.40)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

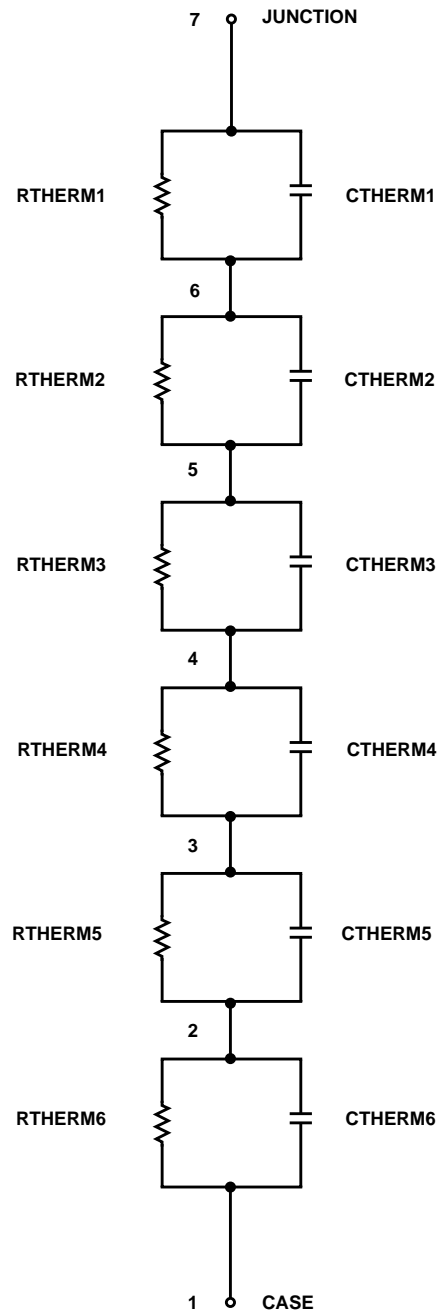
**PSpice Thermal Model**

REV 28 Feb 97

RF1K49224

CTHERM1 7 6 1.00e-7  
 CHERM2 6 5 9.00e-4  
 CHERM3 5 4 3.00e-3  
 CHERM4 4 3 4.00e-2  
 CHERM5 3 2 5.20e-3  
 CHERM6 2 1 1.90e-2

RATHERM1 7 6 7.10e-2  
 RATHERM2 6 5 1.90e-1  
 RATHERM3 5 4 5.95e-1  
 RATHERM4 4 3 4.27  
 RATHERM5 3 2 1.2e1  
 RATHERM6 2 1 1.04e2



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